REMARKS

Claims 1-9, 11-19, 21-36, 38-44, 46-52, 54-59, and 61-69 are currently pending in this application. New claims 70-77 have been added to more particularly point out and define that which Applicant claims has his invention. In particular, new claims 70-77 recited that the design-specific cell is selected from the group consisting of: CMOS cells, static CMOS cells, dynamic CMOS cells and combinations thereof. Support for the various CMOS, static and dynamic cells can be found on pages 5-6 of the Specification.

Applicant expresses his appreciation for the in office interview extended by the Examiner on October 15, 2004, the results of which were summarized in the Interview Summary executed by the Examiner on the same date thereof, wherein the parties reach an agreement with respect to the amendments of independent claims 1, 11, 21, 30, 31, 39, 47 and 54 to more clearly point out and define that which applicant claims as his invention. Applicant presented a Powerpoint presentation which demonstrated that the automated method for designing integrated circuits according to the present invention relates to design-specific cells that are generated, characterized and/or optimized at the transistor level base on design objectives of the integrated circuit rather than conventional automated method for designing cells at the Boolean gate-level. That is, the present invention involves the unique ability to automatically generate, characterize and/or optimized at the transistor-level rather than at the Boolean gate-level level. It was agreed with the Examiner that all of the prior art of record pertained to gate-level design and not at the transistor-level.

Pursuant to the agreement reached with the Examiner, Applicants have amended each independent claim 1, 11, 21, 30, 31, 39, 47 and 54 to clearly point out and define this transistor-level cell creation as demonstrated below in amended claim 1:

Claim 1 – "An automated method for designing integrated circuits, comprising the steps of:

describing an integrated circuit (IC), the description including at least one design objective of said IC;

partitioning said description into at least one functional block, said functional block comprising at least one predefined cell; and

generating at least one design-specific cell representative of said at least one predefined cell of said functional block, wherein said design-specific cell is generated, characterized and/or optimized **at the transistor level** based on said design objective of said IC."

Each of the other independent claims have been similarly amended to recite, *inter alia*, that the design-specific cell is generated, characterized and/or optimized at the transistor level.

Applicant has amended Fig. 3 and the associated specification in order to overcome the objection raised by Office Action in paragraph 3, by removing the narrative from Fig. 3 and inserting on page 16 of the Specification. No new matter has been added, as the text has simply been moved from the figures to the Specification. This objection to Fig. 3 is now moot and should be withdrawn.

Applicant has amended claims 14 and 42 to clarify that it is the steps of characterizing and selecting that are repeated rather than the control module. Accordingly, the objection of claims 14 and 42 is now moot and should be withdrawn.

Applicant has amended claim 67 pursuant to the Examiner's suggestion by replacing criteria with 'design metric'. Accordingly the objection of claim 67 is

now moot and should be withdrawn. Applicant respectfully disagrees with the Examiner's suggestion that claim 68 should depend on claim 67 rather than claim 66. Claim 68 has been amended pursuant to the suggestion of the Examiner to now depend on claim 67. Accordingly, the objection to claim 68 is now moot and show be withdrawn.

Applicant has amended claims 7, 17 and 27 to provide proper antecedent base for the phrase "design metric" and have amended the dependencies of claims 9, 19, and 29, which depend therefrom, respectively. Claims 36 and 52 have been amended to replace the phrase "a criteria" with the phrase "said design metric". Accordingly the rejection of claims 9, 19, 29, 36 and 52 under 35 USC §112, second paragraph, is now moot and should be withdrawn.

Applicant respectfully traverses the rejection of claims 1 and 2 under 35 USC §102(e) as being anticipated by Shubat et al. (Shubat), U.S. Patent No. 6,051,031. As discussed in the Interview held on October 15, 2004, Shubat is directed solely to a method for implementing VLSI designs using a module-based architecture that is based solely on **Boolean gate-level** circuit generation. As clearly set forth in column 4, line 45 through column 5, line 13, Shubat uses a design entry tool and a synthesis program that utilizes a synthesis library in generating Boolean expressions. These Boolean expressions are mapped into a circuit of a single-output Matrix Transistor Logic (MTL) modules. Each MTL module implements one Boolean expression using Pass Transistor Logic technology. Thereafter, each of the modules is constructed.

Applicant respectfully submits that the Boolean gate-level design tool disclosed in Shubat neither describes nor suggests the claimed automated method for designing integrated by, inter alia, partitioning the description into at least one functional block, the functional block comprising at least one predefined cell, and generating at least one design-specific cell representative of the at least one predefined cell of the function block, wherein the design-specific cell is

generated, characterized and/or optimized **at the transistor level** based on the design objective of the IC. Prior to the present invention, Applicants are not aware of any attempts to automatically generate a design-specific cells at the transistor level and Shubat's modules which are generated at the **gate level** neither describe not teach such transistor level cell generation. Moreover, Shubat cannot even optimize the pass-transistor logic structures it creates due to the fundamental architecture of MTL modules.

Applicant respectfully traverses the rejection of claims 1-9, 11-19, 30-36, 38-44, 46, 54-59 and 61-69 under 35 USC §102(e) as being anticipated by Kumashiro et al. (Kumashiro), U.S. Patent No. 6,301,692. Similar to the substantially deficiencies mentioned above with regard to the Shubat patent, Kumashiro, also relates to an automated method for forming an integrated circuit by assembly various Boolean gate-level cells from both a pass-transistor logic layout cell library and a CMOS logic layout cell library. Kumashiro neither describes nor suggests an automated method for designing integrated circuits by, inter alia, partitioning the description into at least one functional block, the functional block comprising at least one predefined cell, and generating at least one design-specific cell representative of the at least one predefined cell of the function block, wherein the design-specific cell is generated, characterized and/or optimized at **the transistor level** based on the design objective of the IC, as recited in the present claims.

Applicant respectfully traverses the rejection of claims 21-29 and 47-52 under 35 USC §102(e) as obvious over Kumashiro. As discussed above, Kumashiro pertains to a method of designing integrated circuits at the gate-level and neither describes nor suggests a design-specific cell produced by, inter alia, partitioning the description into at least one functional block, the functional block comprising at least one predefined cell, and generating at least one design-specific cell representative of the at least one predefined cell of the function block, wherein the design-specific cell is generated, characterized and/or

optimized at the transistor level based on the design objective of the IC, as recited in claims 21-29 and 47-52 of the present invention.

Applicant respectfully requests reconsideration and allowance of the application.

Respectfully submitted,

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AMENDMENTS TO THE DRAWINGS

Applicant has attached hereto a replacement sheet pertaining to the amendments to Fig. 3, as requested by the Examiner on page 2 of the outstanding Office Action.